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MODELS

**PCIe-IDIO-24, PCIe-IDI-24,
PCIe-IDO-24, PCIe-IDIO-12**

**ISOLATED DIGITAL INPUT
FET OUTPUT BOARDS**

USER MANUAL

File: MPCle-IDIO-24.A3e

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ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A BOARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING BOARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O BOARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

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Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

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If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

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Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

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Chapter 1: Introduction

The PCIe-IDIO-24 provides isolated digital inputs with Change of State Detection and isolated FET high-side switches. The board has twenty four optically-isolated input circuits for AC or DC control signals and twenty four isolated FET high-side switches. The board occupies sixteen consecutive addresses in I/O space. Read and write operations may be 8, 16, or 32 bits wide. Several versions of this board are available. The PCIe-IDIO-24 also has eight TTL level non-isolated I/O lines. Model PCIe-IDIO-12 provides twelve isolated inputs and outputs and four TTL/CMOS I/O lines.

Features

- 24 optically isolated, non-polarized digital inputs
 - Software configurable filters on inputs for electrically noisy environments
 - 2 optically isolated groups (common return per 12 channels)
 - Can detect input state change and assert interrupt
- 8 non-isolated TTL/CMOS I/O lines
- 24 optically isolated high-side FET switches
 - 4 groups, sharing external power and return per 6 output channels
- Opto-couplers rated for 2.5kV isolation
- Automatically detected under Windows

Applications

These boards are especially useful in applications where high common-mode external voltages are present. Isolation is required to guard electronics from transient voltage spikes and offers greater common-mode noise rejection in electronically noisy surroundings containing industrial machinery and inductive loads. These applications include factory automation, energy management, industrial ON/OFF control, security systems, manufacturing test, and process monitoring. In addition to protecting industrial applications from accidental contact with high external voltages, the isolation provided eliminates troublesome ground loops.

Functional Description

Inputs

The isolated inputs can be driven by either AC or DC signals. Input signals are rectified by photocoupler diodes. A 1.8K-ohm resistor in series dissipates unused power. Standard 12/24 AC control transformer outputs can be accepted as well as DC voltages. The high input voltage range is 3 to 31 volts (rms). External resistors connected in series may be used to extend the input voltage, however this will raise the input threshold range. Consult with the factory for available modified input ranges.

Each input bank (12x2) contains a switchable filter that has a 4.7 millisecond time constant. Without filtering, rise time response is 10us fall time is 30us. The filter must be selected for AC inputs in order to eliminate the on/off response to the AC zero crossing. The filter is also valuable for use with slow DC input signals in a noisy environment. The filters may be switched out for DC inputs in order to obtain faster response. Filters are selected by the user's software.

Interrupts

When configured by the user's software, the board asserts an interrupt whenever any enabled inputs change state from HIGH (more than 3V) to LOW (less than 1.2V), LOW to HIGH, or both. This is called Change-of-State (COS) detection. See the programming section for a discussion of the COS interrupt management scheme.

Outputs

The solid state outputs are comprised of twenty four fully protected FET high-side switches. The FETs have built in current limiting and are protected against short-circuit, over-temperature, ESD and inductive load transients. The current limitation is activated until the thermal protection acts. The FETs are all off at power-on.

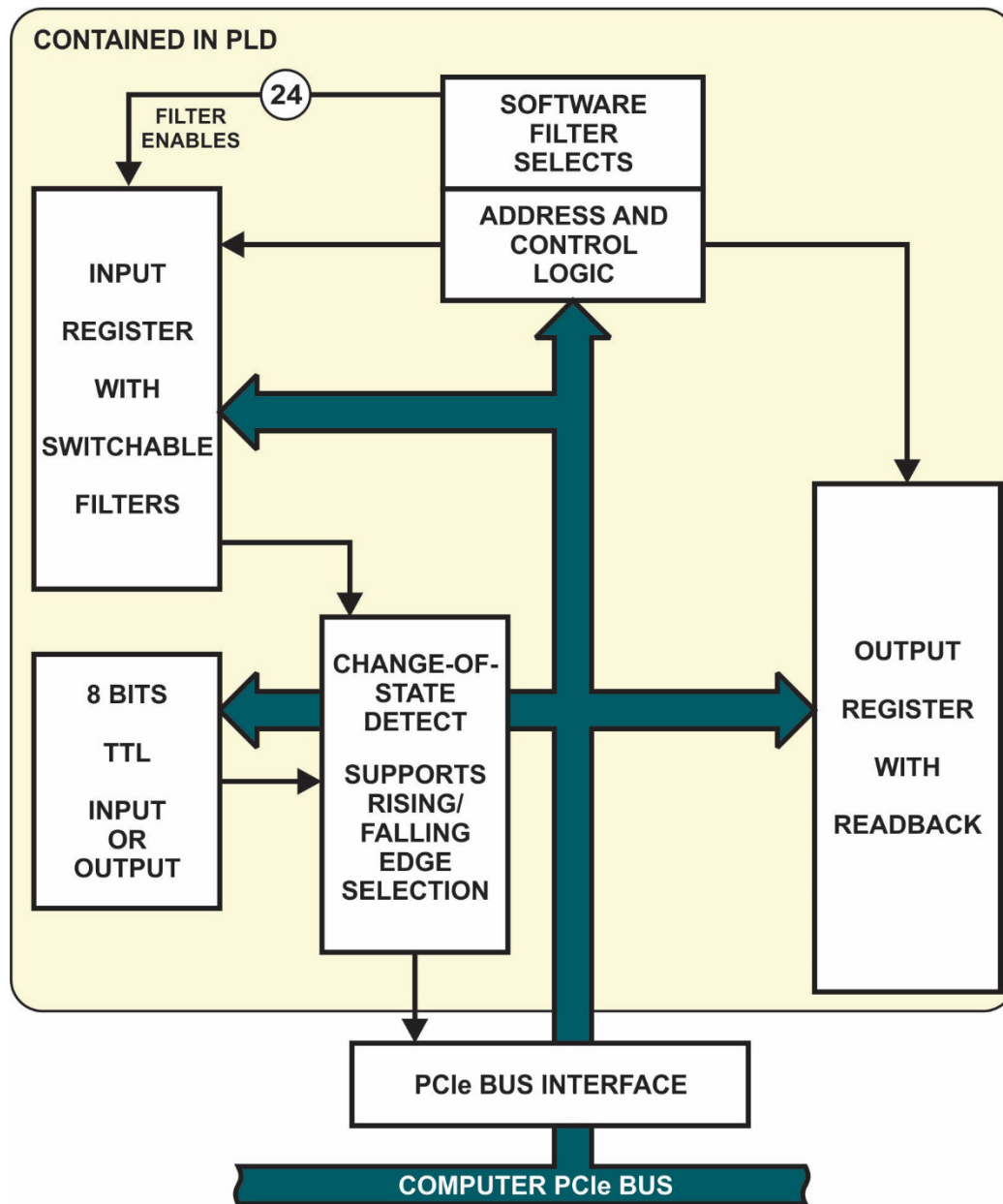


Figure 1-1: Block Diagram

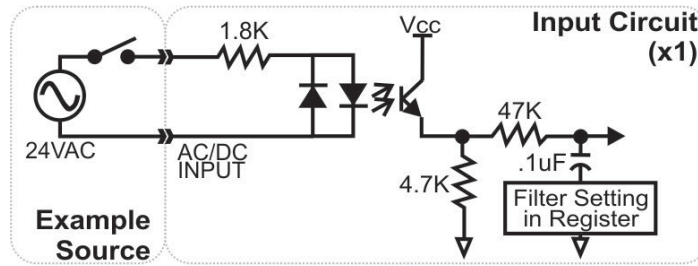


Figure 1-2: Example of One Input Circuit (shared return pin per 12 channel group)

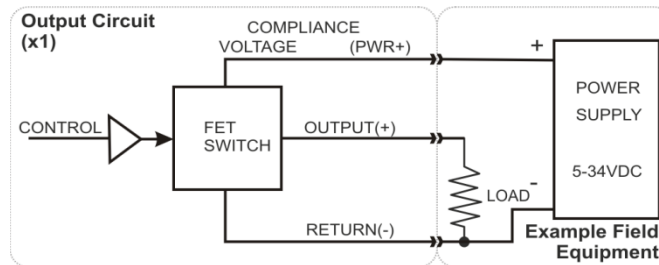


Figure 1-3: Example of One Output Circuit (shared PWR+ and RETURN- pins per 6 channel group)

Note: FETs have two output states: Off, where the output is high impedance (no current flows between the VBB and the output — except for the FET's leakage current, amounting to a few μA), and On, where VBB is connected to the output pin. Therefore, if no load is connected the FET output will have a high floating voltage (due to the leakage current and no path to the VBB switching voltages return). To mitigate this, please add a load to ground at the output.

Ordering Guide

PCIe-IDIO-24	24 isolated inputs 8 non-isolated inputs, 24 high-side FET outputs
PCIe-IDI-24	Inputs only (24 isolated, 8 TTL/CMOS)
PCIe-IDO-24	24 isolated FET outputs and 8 TTL/CMOS I/O lines
PCIe-IDIO-12	12-isolated inputs, 4 TTL I/O lines, 12-isolated outputs

Model Options

-T	Extended temperature (-40° to +85°C)
-RoHS	RoHS compliant version

Included with your board

The following components are included with your shipment. Please take time now to ensure that no items are damaged or missing.

1. Software Master CD (PDF user manual installed with product package)
2. Printed I/O Quick-Start Guide

Optional Accessories

STB-37/2 Kit	Complete screw termination solution, consisting of:
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Two (2) STB-37's installed on a 12" SNAP-TRACK & 6' "Y" Cable Assembly terminating in two DB37F connectors

STB-37/2 Kit-CL Includes four clips for mounting the STB-37/2 Kit to a standard DIN-Rail.

Chapter 2: Installation

Software CD Installation

The software provided with this board is contained on one CD and ***must be installed onto your hard disk prior to use***. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your drive where you see D: in the examples below.

Windows

- a. Place the CD into your CD-ROM drive.
- b. The install program automatically run. If the install program does not run, click START | RUN and type `D:\INSTALL`, click OK or press `Enter`.
- c. Follow the on-screen prompts to install the software for this board.

Linux

- a. Please refer to linux.htm on the CD for information on installing under Linux.

Hardware Installation

Please install the software package before plugging the hardware into the system. Refer to the printed I/O Quick Start Guide included with your board which can also be found on the CD, for specific, quick steps, to complete the hardware and software installation.

Caution! ESD

A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface **prior to touching the card.**

Chapter 3: Hardware Details

Option Selection

There are no jumpers or switches to set or configure prior to installing the card into the PCIe slot of the PC.

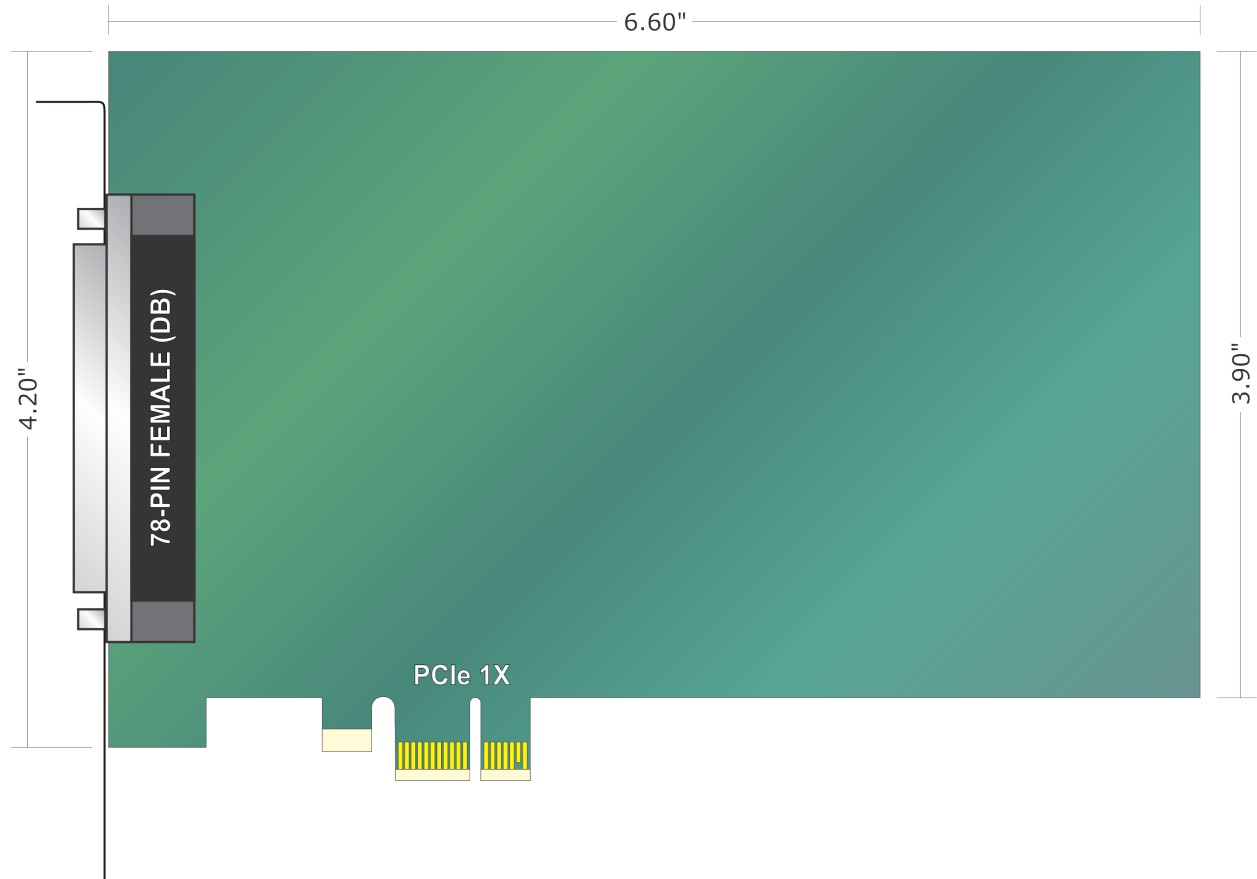


Figure 3-1: Dimensioned Drawing

Chapter 4: Address Selection

The Vendor ID for this card is 0x494F. (ASCII for "IO")
The Device ID for the PCIe-IDIO-24 is 0x0FD0.
The Device ID for the PCIe-IDI-24 is 0x0BD0.
The Device ID for the PCIe-IDO-24 is 0x07D0.
The Device ID for the PCIe-IDIO-12 is 0x0FC0.

This card uses I/O addresses offset from the Offset assigned by the PCIe bus. The address spaces are defined in the programming section of this manual.

PCIe architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCIe cards rather than the user selecting those resources with switches or jumpers. As a result, you cannot set or change the card's Offset or IRQ level. You can only determine what the system has assigned.

The following information is for advanced users only:

The PCIe bus supports 64K of I/O address space, so your card's addresses may be located anywhere in the 0000h to FFFFh range.

The card uses more resources than you usually need be concerned with.

For those who require it, be aware of the following:

BAR[0]: memory mapped PEX8311

BAR[1]: I/O mapped PEX8311

BAR[2]: I/O mapped card registers (←all most software needs)

Chapter 5: Programming

The base or starting address is assigned by the computer system during installation and will fall on a sixteen-byte boundary. The card's readable and programmable registers are as follows:

I/O Address	Read	Write
Base +0	FET Outputs 0-7	FET Outputs 0-7
Base +1	FET Outputs 8-15	FET Outputs 8-15
Base +2	FET Outputs 16-23	FET Outputs 16-23
Base +3	TTL/CMOS 0-7	TTL/CMOS 0-7
Base +4	Isolated Inputs 0-7	Reserved
Base +5	Isolated Inputs 8-15	Reserved
Base +6	Isolated Inputs 16-23	Reserved
Base +7	TTL/CMOS 0-7	Reserved
Base +8	COS Status Inputs 0-7	COS Clear Inputs 0-7
Base +9	COS Status Inputs 8-15	COS Clear Inputs 8-15
Base +A	COS Status Inputs 16-23	COS Clear Inputs 16-23
Base +B	COS Status TTL/CMOS 0-7	COS Clear TTL/CMOS 0-7
Base +C	Control Register	Control Register
Base +D	Reserved	Reserved
Base +E	COS Enable	COS Enable
Base +F	IRQ Output Pin Status	Software Board Reset

Table 5-1: Register Map

Offset +0 (read/write) FET Outputs 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Reading from this address will return the values last written. Writing a 1 to any bit will turn on the corresponding FET output. The card initializes with all outputs off (all “0’s”).

Offset +1 (read/write) FET Outputs 8-15

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8

Reading from this address will return the values last written. Writing a 1 to any bit will turn on the corresponding FET output. The card initializes with all outputs off (all “0’s”).

Offset +2 (read/write) FET Outputs 16-23

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT23	OUT22	OUT21	OUT20	OUT19	OUT18	OUT17	OUT16

Reading from this address will return the values last written. Writing a 1 to any bit will turn on the corresponding FET output. The card initializes with all outputs off (all “0’s”).

Offset +3 (read/write) TTL/CMOS 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0

The card initializes in the Input mode, standard TTL/CMOS levels apply. When Output mode is set (see Offset +C, Control Register), data bit values written will be reflected at the corresponding connector pin, (positive logic).

Offset +4 (read) Isolated Inputs 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Reading from this address will return the Input values. Each bit returning a “1” indicates the corresponding Input is active / energized (from 3V to 31V).

Offset +5 (read) Isolated Inputs 8-15

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8

Reading from this address will return the Input values. Each bit returning a “1” Indicates the corresponding Input is active / energized (from 3V to 31V).

Offset +6 (read) Isolated Inputs 16-23

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN23	IN22	IN21	IN20	IN19	IN18	IN17	IN16

Reading from this address will return the Input values. Each bit returning a “1” Indicates the corresponding Input is active / energized (from 3V to 31V).

Offset +7 (read) TTL/CMOS 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0

Reading from this address will return the Input values. Each bit returning a “0” Indicates the corresponding Input is Low (all Inputs are pulled up to 5V via 10kΩ).

Offset +8 (read) COS Status Inputs 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Reading from this address will return a “1” at each bit for the corresponding Input that has changed state (since the last “Clear” write to Base +8).

Offset +8 (write) COS Clear Inputs 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Writing a “1” to any bit at this address will clear the change of state detection for the corresponding Input, and will also clear the card’s Interrupt Output pin *.

Offset +9 (read) COS Status Inputs 8-15

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8

Reading from this address will return a “1” at each bit for the corresponding Input that has changed state (since the last “Clear” write to Base +9).

Offset +9 (write) COS Clear Inputs 8-15

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8

Writing a “1” to any bit at this address will clear the change of state detection for the corresponding Input, and will also clear the card’s Interrupt Output pin *.

Offset +A (read) COS Status Inputs 16-23

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN23	IN22	IN21	IN20	IN19	IN18	IN17	IN16

Reading from this address will return a “1” at each bit for the corresponding Input that has changed state (since the last “Clear” write to Base +A).

Offset +A (write) COS Clear Inputs 16-23

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN23	IN22	IN21	IN20	IN19	IN18	IN17	IN16

Writing a “1” to any bit at this address will clear the change of state detection for the corresponding Input, and will also clear the card’s Interrupt Output pin *.

Offset +B (read) COS Status TTL/CMOS 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0

Reading from this address will return a “1” at each bit for the corresponding Input that has changed state (since the last “Clear” write to Base +B).

Offset +B (write) COS Clear TTL/CMOS 0-7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0

Writing a “1” to any bit at this address will clear the change of state detection for the corresponding Input, and will also clear the card’s Interrupt Output pin*.

***= If all 32 COS status bits have been cleared)**

Offset +C (read/write) Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	FILTER EN IN12-23	FILTER EN IN0-11	OUT MODE TTL 0-7	BUFFER EN TTL 0-7

Reading from this address will return the values last written. Writing a 1 to any bit will enable the corresponding function.

The card initializes with Bit 0=1 (Enabled), and Bit 1-7=0 (Disabled).

Offset +D Reserved

Offset +E (read/write) COS Enable Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ EN Falling Edge TTL0-7	IRQ EN Falling Edge IN16-23	IRQ EN Falling Edge IN8-15	IRQ EN Falling Edge IN0-7	IRQ EN Rising Edge TTL0-7	IRQ EN Rising Edge IN16-23	IRQ EN Rising Edge IN8-15	IRQ EN Rising Edge IN0-7

Reading from this address will return the values last written. Writing a 1 to any bit will enable the corresponding function.

The card initializes with all bits=0 (COS IRQ disabled).

Offset +F (read) IRQ Output Pin Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	IRQ

Reading from this address will return a "1" at Bit 0 when the card's interrupt pin is active.

Offset +F (write) Software Board Reset

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

Writing any value to this address will return the Control Register to the default state, all Outputs to off, and clear all Input COS status bits.

Interrupts:

The card supports interrupts. The interrupt level is assigned by the plug-and-play operating system. The card's interrupt capability makes it unnecessary to continuously poll inputs.

1. To enable interrupts, SET the appropriate bit(s) in the 8-bit COS Enable Register at offset +E.
 - a. Each bit maps to a group of eight inputs as described above.
 - b. Each group of eight can be configured to generate a COS IRQ on either the rising transition, the falling transition, or both.
2. Read the 4 byte (32 bit) block beginning at offset+8 to see what inputs have changed.
3. If interrupts were enabled and if any of the bits in the block are SET then an IRQ will be generated.
4. To clear interrupts, write the value read from the 32-bit COS-Status register at offset +8, to the 32-bit COS-Clear register at offset +8. This technique will clear the COS latch only for those bits your software has successfully detected as having changed, while allowing other bits to generate COS states in the time between the Status Read, and the COS Clear.

Chapter 6: Connector Pin Assignments

Digital I/O signals are connected to the card via a female 78-pin D type connector that extends through the back of the computer case. The mating connector is an AMPLIMITE 1658674-1 or equivalent. We optionally provide a breakout cable that divides the 78-pin I/O connector down to two female 37-pin D type connectors. See the following pages for information about termination solutions.

Pin	Name	Pin	Name
1	IN_COMMON0	40	IN_COMMON0
2	IN0	41	IN6
3	IN1	42	IN7
4	IN2	43	IN8
5	IN12	44	IN18
6	IN13	45	IN19
7	IN14	46	IN20
8	+5V	47	+5V
9	TTL0	48	TTL4
10	TTL2	49	TTL6
11	VBB0-	50	VBB2-
12	OUT4	51	OUT16
13	OUT2	52	OUT14
14	OUT0	53	OUT12
15	VBB1-	54	VBB3-
16	OUT10	55	OUT22
17	OUT8	56	OUT20
18	OUT6	57	OUT18
19	VBB0+	58	VBB2+
20	VBB0+	59	VBB2+
21	IN3	60	IN9
22	IN4	61	IN10
23	IN5	62	IN11
24	IN15	63	IN21
25	IN16	64	IN22
26	IN17	65	IN23
27	IN_COMMON1	66	IN_COMMON1
28	GND	67	GND
29	TTL1	68	TTL5
30	TTL3	69	TTL7
31	OUT5	70	OUT17
32	OUT3	71	OUT15
33	OUT1	72	OUT13
34	No Connection	73	No Connection
35	OUT11	74	OUT23
36	OUT9	75	OUT21
37	OUT7	76	OUT19
38	VBB1+	77	VBB3+
39	VBB1+	78	VBB3+

Table 6-1: DB78F Pin Assignments (J2) for Model PCIe-IDxx-24

Signal Name	I/O	Signal Description Name
IN_COMMON0	In	Common Return for IN0 thru IN11
IN0 thru IN11	In	Isolated Inputs, 3 to 31VDC or VACrms
IN_COMMON1	In	Common Return for IN12 thru IN23
IN12 thru IN23	In	Isolated Inputs, 3 to 31VDC or VACrms
TTL0 thru TTL7	I/O	5V Logic, Pulled up via 10kΩ
+5V	Out	Unfused +5V connection
GND	Out	+5V and TTLx Return connection
VBB0+	In	Common External Supply + connection for OUT0 thru OUT5
VBB0-	In	Common External Supply - connection for OUT0 thru OUT5
OUT0 thru OUT5	Out	Switched VBB0+ High Side FET Outputs
VBB1+	In	Common External Supply + connection for OUT6 thru OUT11
VBB1-	In	Common External Supply - connection for OUT6 thru OUT11
OUT6 thru OUT11	Out	Switched VBB1+ High Side FET Outputs
VBB2+	In	Common External Supply + connection for OUT12 thru OUT17
VBB2-	In	Common External Supply - connection for OUT12 thru OUT17
OUT12 thru OUT17	Out	Switched VBB2+ High Side FET Outputs
VBB3+	In	Common External Supply + connection for OUT18 thru OUT23
VBB3-	In	Common External Supply - connection for OUT18 thru OUT23
OUT18 thru OUT23	Out	Switched VBB3+ High Side FET Outputs

Table 6-2: I/O Signal Names, Directions and Descriptions

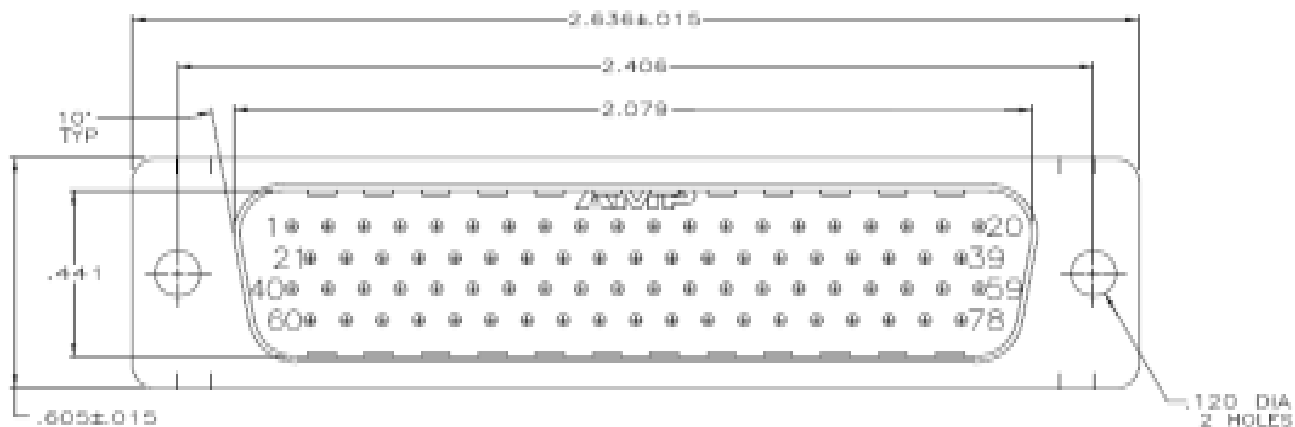


Figure 6-1: DB78M (Mating) Connector

Termination Solutions

The breakout solution involves a “Y” cable that terminates into two identically pinned out DB37F connectors. As part of a kit, these connectors plug into the STB-37 screw terminal cards, which easily mount into a length of SNAPTRACK. The “Y” cable is six (6) feet long on each leg.

PIN	NAME	PIN	NAME
1	IN_COMMON0	1	IN_COMMON0
2	IN0	2	IN6
3	IN1	3	IN7
4	IN2	4	IN8
5	IN12	5	IN18
6	IN13	6	IN19
7	IN14	7	IN20
8	+5V	8	+5V
9	TTL0	9	TTL4
10	TTL2	10	TTL6
11	VBB0-	11	VBB2-
12	OUT4	12	OUT16
13	OUT2	13	OUT14
14	OUT0	14	OUT12
15	VBB1-	15	VBB3-
16	OUT10	16	OUT22
17	OUT8	17	OUT20
18	OUT6	18	OUT18
19	VBB0+	19	VBB2+
20	IN3	20	IN9
21	IN4	21	IN10
22	IN5	22	IN11
23	IN15	23	IN21
24	IN16	24	IN22
25	IN17	25	IN23
26	IN_COMMON1	26	IN_COMMON1
27	GND	27	GND
28	TTL1	28	TTL5
29	TTL3	29	TTL7
30	OUT5	30	OUT17
31	OUT3	31	OUT15
32	OUT1	32	OUT13
33	No Connection	33	No Connection
34	OUT11	34	OUT23
35	OUT9	35	OUT21
36	OUT7	36	OUT19
37	VBB1+	37	VBB3+

Table 6-3: DB37F x 2 Pin Assignments for model PCIe-IDxx-24 only

Pin	Name	Pin	Name
1	IN_COMMON0	40	No Connection
2	IN0	41	No Connection
3	IN1	42	No Connection
4	IN2	43	No Connection
5	IN8	44	No Connection
6	IN9	45	No Connection
7	IN10	46	No Connection
8	+5V	47	+5V
9	TTL0	48	No Connection
10	TTL2	49	No Connection
11	VBB0-	50	No Connection
12	OUT4	51	No Connection
13	OUT2	52	No Connection
14	OUT0	53	No Connection
15	VBB1-	54	No Connection
16	OUT10	55	No Connection
17	OUT8	56	No Connection
18	OUT6	57	No Connection
19	VBB0+	58	No Connection
20	VBB0+	59	No Connection
21	IN3	60	No Connection
22	IN4	61	No Connection
23	IN5	62	No Connection
24	IN11	63	No Connection
25	IN6	64	No Connection
26	IN7	65	No Connection
27	IN_COMMON1	66	No Connection
28	GND	67	GND
29	TTL1	68	No Connection
30	TTL3	69	No Connection
31	OUT5	70	No Connection
32	OUT3	71	No Connection
33	OUT1	72	No Connection
34	No Connection	73	No Connection
35	OUT11	74	No Connection
36	OUT9	75	No Connection
37	OUT7	76	No Connection
38	VBB1+	77	No Connection
39	VBB1+	78	No Connection

Table 6-4: DB78F Pin Assignments for Model PCIe-IDIO-12

Signal Name	I/O	Signal Description Name
IN_COMMON0	In	Common Return for IN0 thru IN5
IN0 thru IN11	In	Isolated Inputs, 3 to 31VDC or VACrms
IN_COMMON1	In	Common Return for IN6 thru IN11
IN12 thru IN23	In	Isolated Inputs, 3 to 31VDC or VACrms
TTL0 thru TTL7	I/O	5V Logic, Pulled up via 10k Ω
+5V	Out	Unfused +5V connection
GND	Out	+5V and TTLx Return connection
VBB0+	In	Common External Supply + connection for OUT0 thru OUT5
VBB0-	In	Common External Supply - connection for OUT0 thru OUT5
OUT0 thru OUT5	Out	Switched VBB0+ High Side FET Outputs
VBB1+	In	Common External Supply + connection for OUT6 thru OUT11
VBB1-	In	Common External Supply - connection for OUT6 thru OUT11

Table 6-5: I/O Signal Names, Directions and Descriptions for Model PCIe-IDIO-12

The breakout solution for the PCIe-IDIO-12 consists of a DB78M to DB37F cable. As part of a kit, the DB37F plugs into an STB-37 screw terminal card, which easily mount into a length of SNAPTRACK. The cable is six (6) feet long.

PIN	NAME
1	IN_COMMON0
2	IN0
3	IN1
4	IN2
5	IN8
6	IN9
7	IN10
8	+5V
9	TTL0
10	TTL2
11	VBB0-
12	OUT4
13	OUT2
14	OUT0
15	VBB1-
16	OUT10
17	OUT8
18	OUT6
19	VBB0+
20	IN3
21	IN4
22	IN5
23	IN11
24	IN6
25	IN7
26	IN_COMMON1
27	GND
28	TTL1
29	TTL3
30	OUT5
31	OUT3
32	OUT1
33	No Connection
34	OUT11
35	OUT9
36	OUT7
37	VBB1+

Table 6-6: DB37F Pin Assignments for Model PCIe-IDIO-12

Chapter 7: Specification

Isolated Digital Inputs

Number of inputs:	24
Type:	Non-polarized, optically isolated sharing a common return per 12 channel input group. (not TTL/CMOS compatible)
Voltage Range:	3 to 31V DC or VACrms (40-10kHz). See note 1
Isolation:	Opto-couplers rated at 2.5kV See note 2
Input Resistance:	1.8k ohms in series with two diodes and a photo-coupler LED
Response Time:	
with filter:	4.7 mSec
without filter:	rise time = 10 uSec; fall time = 30 uSec

Note 1: The design specs a minimum voltage of 3V for the isolated input to comply with the optocoupler's test conditions, ensuring operation within the specified input current range. This approach enables accurate measurement of the Current Transfer Ratio (CTR), minimizes input power consumption, and ensures safe operation during use. While a voltage of around 2V may also generate a high signal, the exact threshold can vary between boards due to component tolerances. The maximum input voltage is 31VDC / VACrms due to the 1/2 watt current-limiting resistor. The design specs the maximum voltage that will be detected as "low" as 1.2VDC. Values between 1.2 and 3VDC are in the hysteresis range.

Non-Isolated Digital Input/Outputs

Number of lines:	8, programmable as all inputs or all outputs
Type:	TTL/CMOS compatible, pulled up to 5V via 10k Ω

Interrupts	Change of State Detection available on all 32 input bits; software enabled byte-by-byte
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Solid State FET Outputs

Number of outputs:	24, isolated in four, 6-channel groups
Output Type:	Smart High Side Power MOSFET Switch Protected against short circuit, over-temp., ESD, can drive inductive loads.
Voltage Range:	5-34VDC recommended (40VDC absolute maximum)
FET Ratings:	On-state resistance = 60m Ω 0.5A continuous per FET, with a 2.5A cumulative total per group of 6 FETs
Leakage Current:	5 μ A maximum

Environmental

Operating Temp.:	0° to 70°C, optional -40° to +85°C
Storage Temp.:	-40 to +85°C
Humidity:	5 to 90 percent (non-condensing)

Mechanical

Size:	Standard height 4.2" (106.65 mm), half-length 6.6" (167.6 mm)
Connector:	DB78 Female
Mating Connector:	AMPLIMITE 1658674-1 or equivalent

Note 2: Opto-couplers are rated for at least 2.5kV, but isolation voltage breakdowns will vary and is affected by factors like cabling, spacing of pins, spacing between traces on the PCB, humidity, dust and other environmental factors. This is a safety issue so a careful approach is required. For CE certification on the front end of the circuitry, isolation was specified at 40V AC and 60V DC. The design intention was to eliminate the influence of common mode. Use proper

wiring techniques to minimize voltage between channels and to ground. For example, when working with AC voltages do not connect the hot side of the line to an input. Tolerance of higher isolation voltage can be obtained on request by applying a conformal coating to the board.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accessio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.



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